1. A method of operating a processor comprising:
concatenating a first word and a second word to produce an intermediate result;
shifting the intermediate result by a specified shift amount; and
storing the shifted intermediate result in a third word.

2. The method of claim 1 wherein the first word and the second word and the third word are 32-bit words.

3. The method of claim 1 wherein the intermediate result is a 64-bit word.

4. The method of claim 1 wherein shifting comprises right shifting.

5. The method of claim 4 wherein the specified shift amount is in an operand.

6. The method of claim 4 wherein the specified shift amount is a value between one and thirty-one.

7. The method of claim 4 wherein the specified shift amount is a value contained in a lower five bits of the first word.

8. A computer instruction comprising:
an instruction to concatenate a first word and a second word to produce an intermediate result;
shift the intermediate result by a specified amount; and
store the shifted intermediate result in a third word.

9. The instruction of claim 8 wherein the first word and the second word and the third word are 32-bit words.

10. The instruction of claim 8 wherein the intermediate result is a 64-bit word.

11. The instruction of claim 8 wherein shifting comprises right shifting.

12. The instruction of claim 11 wherein the specified amount is in an operand.

13. The instruction of claim 11 wherein the specified amount is a value between one and thirty-one.

14. The instruction of claim 11 wherein the specified amount is a value contained in a lower five bits of the first word.

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